IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method for detecting transfer errors in an address bus, comprising:

generating a first address parity using a memory address;

scrambling at least two data error-correction-code (ECC) check bits using the first address parity; and

writing the data ECC check bits to a memory, the data ECC check bits enabling detection of transfer errors in the address bus;

generating a second address parity using the memory address;

reading the data ECC check bits from the memory; and

unscrambling the at least two data ECC check bits using the second address parity, the data ECC check bits enabling detection of transfer errors in the address bus;

wherein the method operation of unscrambling the at least two data ECC check bits is selected from one of using an exclusive-OR function and using an exclusive-NOR function.

2. (Cancel)

3. (Currently amended) The method of claim 1 [[2]], further comprising:

executing an ECC operation; and

reporting an ECC error to an exception-handling software if the at least two data ECC check bits signal an error.

4.-5. (Cancelled)

6. (Previously presented) A method for detecting transfer errors in an address bus, comprising:

generating a first address parity using a memory address;

scrambling at least two data error-correction-code (ECC) check bits using the first address parity; and

writing the data ECC check bits to a memory, the data ECC check bits enabling detection of transfer errors in the address bus;

wherein the at least two data ECC check bits are selected from the group consisting of two most significant bits and two least significant bits.

7. (Previously presented) A method for detecting transfer errors in an address bus, comprising:

generating a second address parity using a memory address;

reading data error-correction-code (ECC) check bits from the memory; and

unscrambling at least two previously scrambled data ECC check bits using the second address parity, the data ECC check bits enabling detection of transfer errors in the address bus;

executing an ECC operation; and

reporting an ECC error to an exception-handling software if the at least two previously scrambled data ECC check bits signal an error.

8. (Cancelled)

9. (Previously presented) A method for detecting transfer errors in an address bus, comprising:

generating a second address parity using a memory address;

reading data error-correction-code (ECC) check bits from the memory; and

unscrambling at least two previously scrambled data ECC check bits using the second address parity, the data ECC check bits enabling detection of transfer errors in the address bus;

wherein the method operation of unscrambling the at least two previously scrambled data ECC check bits is selected from one of using an exclusive-OR function and using an exclusive-NOR function.

10. (Previously presented) A method for detecting transfer errors in an address bus, comprising:

generating a second address parity using a memory address;

reading data error-correction-code (ECC) check bits from the memory; and

unscrambling at least two previously scrambled data ECC check bits using the second address parity, the data ECC check bits enabling detection of transfer errors in the address bus;

wherein the at least two previously scrambled data ECC check bits are selected from the group consisting of two most significant bits and two least significant bits.

11.-17. (Cancelled).